4. (Original) The logic unit of claim 3, wherein the one transistor comprises an insulated-gate field-effect transistor.

5. (Original) The logic unit of claim 4, wherein the insulated-gate field-effect transistor comprises a *p-type* insulated-gate field-effect transistor.

6. (Original) The logic unit of claim 1, wherein the voltage-level converter comprises an inverter.

7. (Original) The logic unit of claim 6, wherein the inverter comprises an *n-type* insulated-gate field-effect transistor connected in series with the at least one transistor.

8. (Original) The logic unit of claim 6, wherein the second logic unit comprises a clock distribution circuit.

9. (Original) The logic unit of claim 6, where the voltage-level converter comprises a first inverter coupled in series to a second inverter.

10. (Original) The logic unit of claim 9, wherein the first inverter includes the at least one transistor.

11. (Original) A logic unit comprising:

a first logic unit connected to a first supply voltage;

a second logic unit connected to a second supply voltage; and

a logic circuit connecting the first logic unit to the second logic unit, the logic circuit including at least one transistor having a threshold voltage greater than or about equal to the difference between the second supply voltage and the first supply voltage and the at least one transistor connected to the second supply voltage .

12. (Original) The logic unit of claim 11, wherein the logic circuit comprises an AND circuit.

13. (Original) The logic unit of claim 11, wherein the logic circuit comprises a NAND circuit.

14. (Original) The logic unit of claim 11, wherein the logic circuit comprises an OR circuit.

15. (Original) The logic unit of claim 11, wherein the logic circuit comprises a NOR circuit.

16. (Original) The logic unit of claim 11, wherein the logic circuit comprises an XOR circuit.

17. (Original) The logic unit of claim 11, wherein the second logic unit comprises a clock distribution circuit.

18. (Original) The logic unit of claim 17, wherein the logic circuit comprises a NAND circuit.

19. (Original) The logic unit of claim 17, wherein the logic circuit comprises a NOR circuit.

20. (Original) The logic unit of claim 11, wherein the second logic unit comprises an arithmetic unit.

21. (Original) The logic unit of claim 20, wherein the logic circuit comprises an OR circuit.

22. (Original) The logic unit of claim 20, wherein the logic circuit comprises an XOR circuit.

23. (Original) A method comprising:

transmitting a logic signal from a logic unit having an output voltage swing between a first voltage level and a second voltage level, the first voltage being greater than the second voltage level;

receiving the logic signal at a logic circuit having a pull-up transistor and an output voltage swing between a third voltage level and a fourth voltage level, the third voltage being greater than the fourth voltage level; and

turning off the pull-up transistor when the logic signal has a value slightly greater than the difference between the third voltage level and the first voltage level, the third voltage level being greater than the first voltage level.

24. (Original) The method of claim 23, further comprising:

generating an output logic signal at the logic circuit, the output logic signal having a voltage swing between the third voltage level and the fourth voltage level; and

receiving the output logic signal at an inverter having an output voltage swing between the third voltage level and the fourth voltage level.

25. (Original) The method of claim 23, further comprising:

generating an output logic signal at the logic circuit, the output logic signal having a voltage swing between the third voltage level and the fourth voltage level; and

receiving the output logic signal at a logic circuit having an output voltage swing between the third voltage level and the fourth voltage level.